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Review Article

A Review on Low Power Low Noise Amplifier

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A B S T R A C T

In this paper, we are reviewing a fully integrated Electro Static Discharge (ESD)-protected Low-Noise Amplifier (LNA) for low-power and narrowband applications using a cascade inductive source degeneration topology, designed and fabricated in 130-nm CMOS silicon-on-insulator technology. The different designed LNA was operated from a range of 11-dB to 15 db power gain at different frequencies. The Noise figure, input return loss, power consumption & protection level are the major parameter for analysis. An extensive survey of analytical models and experimental results reported in the literature is carried out to quantify the issue of excessive thermal noise for short-channel CMOS. Short channel effects such as channel-length modulation and velocity saturation effects are also accounted for in our optimization process.

Keywords: LNA, CMOS, Bandwidth, Power Gain

Introduction

With advancement in state-of-the-art electronic systems and a huge demand for low-cost high-speed mixed-signal integrated systems, a considerable effort has recently been made to migrate several high-frequency elementary circuit blocks from GaAs to the CMOS silicon process. Since CMOS Silicon-On-Insulator (SOI) devices present a very good high-frequency behavior and low-power consumption, it is of great interest to use them in RF circuit design.[1]

Over the last decade, the MOS transistor channel length scaled down to deep sub micrometer to improve device performance in term of cutoff frequency. Recently, a 130-nm Partially Depleted (PD) SOI CMOS technology with a transit frequency of 243 GHz and maximum frequency of oscillation of 208 GHz has been reported.[2] Such transition frequencies well above 100 GHz offer a comfortable frequency margin for RF designers. Recently, many designs of different RF blocks such as Low-Noise Amplifiers (LNAs), Voltage-Controlled Oscillators (VCOs), and mixers have demonstrated the interest of this technology for low-voltage and low-power applications.

Power consumption is a major concern for high-performance digital systems and portable applications. The most efficient technological approach for reducing power consumption is power-supply voltage scaling. For this purpose SOI devices bring their unique inherent advantages over bulk devices: lower junction capacitance, lower junction leakage, no latch-up, lower sensitivity, and full dielectric isolation.[1]

In a typical radio receiver, the LNA is one of the key components, as it tends to dominate the sensitivity. The LNA design involves many tradeoffs between the Noise Figure (NF), gain, linearity, impedance matching, and power dissipation. Generally, the main goal of LNA design is to achieve simultaneous noise and input matching at any given amount of power dissipation.

Electro Static Discharge (ESD) protection for RF device applications is becoming increasingly important. Traditional ESD protection structures, whether on or off chip, are often responsible for performance degradation of RF blocks. SOI ESD protection networks have already made considerable progress in achieving industry-acceptable ESD protection levels using gated diodes, gate-coupled MOSFETs, and Zener diodes.[3] Introduction of systematic characterization benchmark strategies and new testing techniques (e.g., Transmission Line Pulse (TLP) testing) will allow better understanding of the ESD robustness of advanced technologies.[4]

With the decrease of gate–oxide thickness, CMOS circuits become more sensitive to stress from ESD phenomena. LNA constitutes one of the most critical building blocks in the RF front-end. It is usually connected to the outside world through the antenna and can be exposed to ESD stress. In this study, the performance of 2.4-GHz CMOS SOI LNAs with/ without ESD protection, fully integrated on 130-nm RF SOI CMOS technology, is discussed.

The rest of paper is design as follows. The designing challenges are described in section II receptively. Related literature survey work is described in Section III. Performance parameters are defined in section IV. The overall conclusion of review describe in section V.

Designinig Challenges

Designing wideband LNAs for wireless applications presents two levels of challenges. In the first place, having fast and low noise transistors depends on the available technology. Traditionally, wideband microwave amplifiers relied on transistors realized with composite semiconductors, e.g., GaAs, because of the intrinsic superior frequency characteristics of such devices.[5-7] Silicon technology, on the other hand, has been employed to design and fabricate amplifiers, even wideband ones, for particular applications, e.g., optical communications,[8,9] that require different specifications compared to wireless systems. In wireless mobile communications systems, silicon integrated circuits have been widely employed in narrow-band systems, where limited gain and increased parasitic are tolerable due to lower operating frequencies and the application of tuned networks. There are few examples of development of high-frequency wideband amplifiers employing silicon transistors, in particular in CMOS technology. In this case, it is remarkable that employed solutions (distributed amplifiers)[10-12] require high levels of power consumption, and they are not optimized for noise. This brings about the second challenge-finding a lowpower topology that satisfies all the other design requirements, the most stringent one being the input match. Another possibility is balanced amplifiers. In this case, though, the input match is achieved by means of a resistive termination. This results in a degradation of the overall noise performance, as the minimum achievable NF is 3 dB. Moreover, balanced amplifiers require quadrature hybrid couplers that are either narrow band or, if they are wideband, they are multi sectional and very large. Thus, they are not amenable to integration.

- Power consumption is a very important criterion
- At the same time we need to have a cost effective solution for the problem of constructing RF circuits using non Si Ge technologies
- We need a substitute that can provide the benefits of the Si Ge technology like low power and high gain
- This is one of the reasons why the use of the CMOS technology is increasing in the design of the Low Noise Amplifiers of the RF Front end
- There are certain CMOS designs that consume several tens of milli watts, this approach reduces the power consumption to just a few milli watts

In low noise amplifier, for achieving low noise high amplification is required for the amplifier in first stage. Therefore we required high electron mobility transistors which should be driven in a high current region, which is not a energy efficient and problem also occurring in input and output matching.

Litereture Review

This section will provide the brief description and highlights the contribution, remarks and factors of the work done by the researchers. Many attempts have been made in the past to achieve low power consumption.

In this paper, author told about high pass pole can be formed by the feedback capacity and the pseudo resistance cell. Voltage, gain, noise and fabrication area was achieved upto 1.8 V, 39.98 db, 096 u and 0.065.[1]

In this paper, author told about A floating-gate based reconfigurable OTA-C filter has been designed and implemented. In the proposed power efficient linearized OTA, floating-gate transistors are employed for current bias and common-mode feedback implementation.[2]

Biomedical recording Instrument and Bluetooth Serial plugin for performing serial communication with the HC-05 module. Gain Characteristics improves Frequency Response & Amplified output was evaluated. Peak to peak noise ratio & mean was getted up to 1.52, Mean: 2.40 Bluetooth module is positively paired with other Bluetooth enabled devices and is able to detect these devices within the 100 meter range.[3]

Designing of on chip low-noise and low-power FEA for various neural recording applications. TSMC 0.90nm technology Gain: 39 db, Noise Efficiency Factor: 2.89 and B.W: 5.2 – 540 KHz The designed amplifier not only reduces the input-referred noise but also improves the linearity of the circuit.[4]

Proposed ultra-low power Bio amplifier with feedback circuitry. main concern is to design circuit with ultra-low power consumption, transistors are preferred to be operate in weak inversion region. Gain, Bandwidth and frequency range and power are 45.38 db, 2.9 KHz, 5.02 Hz – 2.927 KHz and 6.25 µ. The designed amplifier not only reduces the input-referred noise but also improves the linearity of the circuit.[5]

In this paper, Acquision Front End Method is used. This work presents two ULP BSA front-ends, BSA I and BSA II. Gain: 39

db PSRR, CMRR, bandwidth was achieved up to 70 db, 74 db and 2-175 Hz The circuit architecture presented in this work can serve as the basis for a highly miniaturized and ultra-low power brain signal acquisition unit for a future fully implantable BCI system.[6]

The system has a pre-amplifier, a high pass function by means of feedback capacitors and resistors, a buffer, and a low pass filter. The Technology, gain, power, bandwidth and voltage was 0.18 µm, 89.9 db, 55.8 µW, 10- 10.9 KHz and 2.19 µV. Although a more modern process has advantages, such as higher speed, lower power consumption, smaller area, etc, advanced process also inherits a larger noise floor.

Table 1.Litereture Review

Authors	Paper Title	Research Methodology used	Major Findings	Research prospects
Yali Su, Xuan Liu	Design of a Low Noise Low Power Preamplifier used for Portable Biomedical Signal Acquisition	A high pass pole can be formed by the feedback capacity and the pseudo resistance cell.	Voltage : 1.8 Gain : 39.98 Noise : 096 u Area : 0.065	The designed preamplifier is suitable for biomedical signal acquisition circuit with low power consumption, low noise and high integration
Sheng-Yu Peng, Yu-Hsien Lee, Tzu-Yun Wang	A Power-Efficient Reconfigurable OTA-C Filter for Low-Frequency Biomedical Applications	A floating-gate based reconfigurable OTA-C filter has been designed and implemented	Input Voltage Range : 216 m Vpp Gm Deviation < 1.56 %. THD : 40 db SFDR : 52.6 db for LPF SFDR : 53.63 db for HPF Power : 303 n W	In the proposed power efficient linearized OTA, floating-gate transistors are employed for current bias and common-mode feedback implementation
Sayali Joshi Asmita wakankar, Dr. Niranjan Khambete	Design & Implementation of Low Power Compact Amplifier Circuitry for Wearable Bio signal Device	Biomedical recording Instrument Bluetooth Serial plugin for performing serial communication with the HC-05 module	Gain Characteristics improves Frequency Response & Amplified output P-P : 1.52 Mean : 2.40	Bluetooth module is positively paired with other Bluetooth enabled devices and is able to detect these devices within the 100 meter range
Richa Dubey, Anjan Kumar, Manisha Pattanaik	Design of Low Noise Bio potential tunable amplifier using Voltage Controlled Pseudo-resistor for Bio signal Acquisition Applications	Designing of on chip low-noise and low-power FEA for various neural recording applications TSMC 0.90nm technology	Gain : 39 db Noise Efficiency Factor : 2.89 B.W : 5.2 – 540 KHz	The designed amplifier not only reduces the input-referred noise but also improves the linearity of the circuit
Pratyusha, Sanjeev Kumar and Anita Kumari	Low Power Amplifier For Bio potential Signal Acquisition System	Proposed ultra low power Bio amplifier with feedback circuitry. Main concern is to design circuit with ultra low power consumption, transistors are preferred to be operate in weak inversion region	Gain : 45.38 db B.W : 2.9 KHz Frequency Range : 5.02 Hz – 2.927 KHz Power : 6.25 µ	Low power circuits are generally preferred for the safety of patients

Alireza Karimi-Bidhendi, Omid Malekzadeh-Arasteh	CMOS Ultralow Power Brain Signal Acquisition Front-Ends: Design and Human Testing	Acquision Front End Method is used. This work presents two ULP BSA front-ends, BSA I and BSA II.	Gain: 39 db PSRR:70 db CMRR: 74 db B.W : 2-175 Hz	The circuit architecture presented in this work can serve as the basis for a highly miniaturized and ultra-low power brain signal acquisition unit for a future fully implantable BCI system
Ming-Ze Li and Kea-Tiong	A Low-Noise Low-Power Amplifier for Implantable Device for Neural Signal Acquisition	The system has a pre-amplifier, a high pass function by means of feedback capacitors and resistors, a buffer, and a low pass filter	Technology : 0.18 µm Gain : 89.9 db Power : 55.8 µW B.W : 10- 10.9 KHz Voltage : 2.19 µV	Although a more modern process has advantages, such as higher speed, lower power consumption, smaller area, etc, advanced process also inherits a larger noise floor

Performance Parameter

The other parameter of LNA with CMOS technology are Gain, noise figure and power respectively.[8] These parameter are as:

The ratio between the signal outputs of a system to signal input of a system is called gain. For LNA design there are three power gain definitions appears in the literature.

- Transducer power gain (GT)
- Operating power gain (GP)
- Available power gain (GA)

Noise figure is commonly used to define extra noise generated by a circuit or system. It can also be said that, the ratio between[17] SNR at input to the SNR at output, and is expressed in decibels. It is expressed by following Equation

$$NF = 10 \log \frac{SNR_{in}}{SNR_{out}}$$

Where

NF= Noise figure

SNR_{in} = Signal to Noise ratio at the input of a circuit or system

SNR_{out} = Signal to Noise ratio of the circuit or system at output.

An amplifier uses electric power from a power supply to increase the amplitude of a signal. The amount of amplification provided by an amplifier is measured by its gain: the ratio of output voltage, current, or power to input. An amplifier is a circuit that has a power gain greater than one.

Conclusion

A fully integrated LNA with an on-chip ESD protection technique was studied. The protected LNA provide high gain & less reflection coefficient. ESD protection solution can be applied to any sub-130-nm RF CMOS technology with thinner gate oxides.

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